

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Chennupati Attorney Docket: 2003 P 50641 US
Filed: Herewith Examiner: TBD
Serial No.: TBD Art Unit: TBD
For: Circuit Module having Interleaved Groups of Circuit Chips

Mail Stop: Patent Application
Commissioner for Patents
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Alexandria, VA 22313-1450

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Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed combined form PTO/SB/08A & 08B that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

Please contact Applicant's attorney at the number listed below with any questions regarding this matter.

Respectfully submitted,



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February 24, 2004

Date

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				Application Number	TBD
				Filing Date	Herewith
				First Named Inventor	Chennupati
				Art Unit	TBD
				Examiner Name	TBD
				Attorney Docket Number	2003 P 50641 US
Sheet	1	of	1		

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